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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/750,389 | 12/31/2003 | Tony Albrecht | 5367-65 | 8976 |

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| EXAMINER | |
|---|---|
| LE, THAO X | |
| ART UNIT | PAPER NUMBER |
| 2814 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
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| 3 MONTHS | 03/01/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/750,389 | ALBRECHT ET AL. | |
| | Examiner | Art Unit | |
| | Thao X. Le | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 December 2006*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7, 22-23 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6693352 to Huang et al.

Regarding claim 1, Huang discloses a light-emitting diode chip in fig. 7 having an epitaxial semiconductor layer sequence 31-35, col. 4 lines 59-64, with an active zone 33, column 4 line 41, that emits electromagnetic radiation and an electrical contact structure comprising: a radiation-transmissive electrical current expansion layer 36A, col. 7 line 19, which contains ZnO, column 8 lines 4-10, and an electrical connection layer 37A/38A, column 4 line 51, wherein the current expansion layer 36A is applied directly on a cladding layer 35, col. 4 line 49, of the semiconductor layer and comprises a window, in which the connection layer 37A/38A is applied directly on said cladding layer 35 of the semiconductor layer sequence, and said cladding layer is P-doped, col. 4 line 48, wherein the connection layer 37A/38A is electrically conductively connected to the current expansion layer 36A, and wherein junction between the connection layer

37A/38A and the cladding layer 34, during the operation of the light-emitting diode chip, is not electrically conductive or is only poorly electrically conductive such that an entire, or virtually the entire, current from the connection layer 37A/38 flows via the current expansion layer 36A into the semiconductor layer sequence, col. 10 lines 42-55.

Regarding claim 2, Huang discloses the light-emitting diode chip according to claim 1, wherein the connection layer 37A/38A comprises a metal, column 5 line 30 or 49, and the junction between the connection layer 37A and the cladding layer 35 comprises an electrical potential barrier, col. 10 line 48.

Regarding claims 3-4 and 22, Huang discloses the light-emitting diode chip according to claim 1, the sheet resistance of intermediate layers of the semiconductor layer sequence between the active zone and the electrical contact structure is greater than or equal to 200 Ω /sq, wherein the current expansion layer 44 comprises a sheet resistance of less than or equal to 190 Ω /sq or 30 Ω/sp.

Although the prior art does not specially disclose the sheet resistance limitation, this feature is seen to be inherently teaching of that limitation because Huang discloses the material and structure substantially identical to claimed invention, claimed properties or functions are presumed to be inherent. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Regarding claim 5, Huang discloses the light-emitting diode chip according to claim 1, wherein the connection layer 37B extends beyond the window on a side of the current expansion layer 36A, which is remote from the semiconductor layer sequence and is applied to a front-side surface of the current expansion layer 36A so that the

junction between the connection layer 37A/38A and the current expansion layer 36A is electrically conductive in this region, fig. 7

Regarding claim 6, Huang discloses the light-emitting diode chip according to claim 1 wherein the semiconductor layer sequence is based on $In_xGa_yAl_{1-x-y}N$ where $0 \leq x \leq 1$, $0 \leq y \leq 1$ and $x + y \leq 1$, col. 4 lines 35-40.

Regarding claims 7 and 23, Huang discloses the light-emitting diode chip according to claim 1 wherein the lading layer 22 comprises $Al_xGa_{1-x}As_yP_{1-y}$ where $0 \leq x \leq 1$, $0 \leq y \leq 1$, col. 9 line 36.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 8-9 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6693352 to Huang et al. in view of US 5717226 to Lee et al.

Regarding claim 8, Huang does not discloses the light-emitting diode chip according to claim 7 wherein the cladding layer is p-doped with at least one of the dopant Zn and C.

However, Lee discloses layer 33 is P-type cladding layer. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to understand that Zn would be a typical material used in the art as a dopant of p-type for cladding layer, see Wang (6469324) column 2 lines 26, Sasaki (6074889) column 1 lines 48-51, or Takeoka (5789773) column 1 line 61.

Regarding claims 9, 24, Huang does not disclose the light-emitting diode chip wherein the layer cladding layer 22 is doped with a dopant concentration of between about $1x10^{18}$

However, Lee discloses the light-emitting diode chip wherein the layer cladding layer 33 is doped with a dopant concentration of between about $1x10^{18}$, column 1 line 46. Accordingly, it would have been obvious to one of ordinary skill in art to use the doping teaching of Lee in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

6. Claims 10-13 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6693352 to Huang et al. in view of US 6346719 to Udagawa et al.

Regarding to claims 10-11, 25-26, Huang does not disclose the current expansion layer 44 comprises Al; and wherein the proportion of Al between 0% and 10% and 1% and 3%.

However, Udagawa discloses the light-emitting diode in fig. 6 wherein the expansion layer 406 comprises Al, column 8 line 56, wherein the proportion of Al between 0% and 10%, column 8 line 57. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the ZnO:Al layer 406 teaching of Udagawa with Huang's device, because Al doped ZnO would have created a specific resistance level for layer ZnO as taught by Udagawa, column 8 line 59.

Regarding claims 12-13, Huang does not disclose the light-emitting diode chip according to claim 1 wherein the current expansion layer has a thickness between 100 and 600 nm, wherein the current expansion layer 44 has a thickness corresponding to about a quarter of a wavelength of a radiation emitted by the light-emitting diode chip.

However, Huang discloses the light-emitting diode chip wherein the current expansion layer 36A has a thickness between 40 nm, col. 5 line 16. Accordingly, it would have been obvious to one of ordinary skill in art to use the doping teaching of Huang in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not

inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

7. Claims 14-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6693352 to Huang et al. in view of JP 2001036131 to Udagawa.

Regarding claims 14-21, Huang does not discloses the light emitting diode wherein the current expansion layer is provided with watertight material such that the current expansion layer is adequately protected against moisture, wherein watertight material is applied to free areas of the contact layer, wherein watertight material is applied to all the free areas of the contact layer, wherein the watertight material is a dielectric that is transparent to an electromagnetic radiation emitted by the light-emitting diode chip, wherein the dielectric comprises one or more of the substances $Si_xN_y$, SiO, $SiO_2$, $Al_2O_3$ and $SiO_xN_y$, wherein a refractive index of the watertight material is less than the refractive index of the current expansion layer and is adapted so as to significantly minimized reflections of the radiation emitted by the light-emitting diode chip at interfaces with respect to the watertight material, wherein the current expansion layer has a thickness corresponding to about an integer multiple of half the wavelength of a radiation emitted by the light-emitting diode chip, and the watertight material has a thickness corresponding to about a quarter of said wavelength, wherein the thickness of the watertight material is in a range of between 50 and 200 nm inclusive.

However, Udagawa discloses the light emitting diode in fig. 1 wherein the current expansion layer 107 is provided with watertight material 108 in such a way that it is adequately protected against moisture, wherein watertight material

is applied to free areas of the contact layer, wherein watertight material 108 is applied to all the free areas of the contact layer, wherein the watertight material 108 is a dielectric that is transparent to an electromagnetic radiation emitted by the light-emitting diode chip, wherein the dielectric comprises one or more of the substances $Si_xN_y$, SiO, $SiO_2$, $Al_2O_3$ and $SiO_xN_y$, see abstract, wherein the refractive index of the watertight material is less than the refractive index of the current expansion layer and is adapted to the greatest possible extent in particular for a minimization of reflections of the radiation emitted by the light-emitting diode chip at interfaces with respect to the watertight material, see abstract, wherein the current expansion layer 107 has a general thickness, wherein the thickness of the watertight material 108 has a general thickness. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the watertight layer teaching of Udagawa with Huang's device, because it would have provided the protection and improved light emitting efficiency as taught by Udagawa, see abstract.

With respect to the thickness, it would have been obvious to one of ordinary skill in art to use the general thickness teaching of Udagawa with Huang's device in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

***Response to Arguments***

8. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

23 Feb. 2007

THAO X. LE
PRIMARY PATENT EXAMINER